Amendments to the Claims

Claim 1 (previously presented): A predistortion circuit for compensating linear distortion introduced by analog-transmitter components of a digital communications transmitter, said predistortion circuit comprising:

a source of a complex-forward-data stream configured to digitally convey information within a bandwidth;

a digital equalizer section coupled to said complex-forward-data-stream source and configured to generate an equalized-complex-forward-data stream and to pass said equalized-complex-forward-data stream to said analog-transmitter components;

a feedback section comprising a complex-digital-subharmonic sampling downconverter adapted to receive a feedback signal from said analog-transmitter components, and configured to provide a complex-return-data stream at greater than or equal to said bandwidth; and

a controller coupled to said feedback section and to said equalizer section and configured so that said equalizer section compensates for frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components.

Claim 2 (original): A predistortion circuit as claimed in claim 1 wherein said analog-transmitter components include a power amplifier having an input and an output, and said feedback section comprises:

a first analog input adapted to receive a first RF-analog signal from said power amplifier input; and

a second analog input adapted to receive a second RF-analog signal from said power amplifier output.

Claim 3 (original): A predistortion circuit as claimed in claim 2 wherein said controller is configured to compensate for

linear distortion in an RF-analog signal present at said input of said power amplifier, then compensate for linear distortion in an amplified RF signal present at said output of said power amplifier.

Claim 4 (original): A predistortion circuit as claimed in claim 1 wherein said equalizer section comprises:

a non-adaptive equalizer configured to be programmed with filter coefficients; and

an adaptation engine coupled to said non-adaptive equalizer and configured to implement an estimation-and-convergence algorithm which determines said filter coefficients.

Claim 5 (original): A predistortion circuit as claimed in claim 4 wherein said non-adaptive equalizer processes said complex-forward-data stream, and said adaptation engine is responsive to said complex-forward-data stream and said complex-return-data stream.

Claim 6 (original): A predistortion circuit as claimed in claim 4 wherein:

said non-adaptive equalizer is a complex equalizer having an in-phase path, a quadrature path, an in-phase-to-quadrature path, and a quadrature-to-in-phase path;

a first set of said filter coefficients is programmed in said in-phase and quadrature paths, and a second set of said filter coefficients is programmed in said in-phase-to-quadrature and quadrature-to-in-phase paths; and

said adaptation engine accommodates a partial complex equalizer and has first and second paths, said first and second paths being configured in one mode to determine said filter coefficients for said in-phase and quadrature paths, and being configured in another mode to determine said filter coefficients for said in-phase-to-quadrature and quadrature-to-in-phase paths.

Claim 7 (original): A predistortion circuit as claimed in claim 1 wherein said equalizer section implements an estimation-and-convergence algorithm to determine filter coefficients that compensate for said frequency dependent quadrature gain and phase imbalance.

Claim 8 (original): A predistortion circuit as claimed in claim 7 wherein:

said estimation-and-convergence algorithm is responsive to said complex-forward-data stream and to said complex-return-data stream;

said complex-forward-data stream and said complex-return-data stream exhibit forward-error and return-error levels, respectively, with said return-error level being greater than said forward-error level; and

said estimation-and-convergence algorithm is configured to transform increased algorithmic processing time into reduced effective-error level for said complex-return-data stream.

Claim 9 (original): A predistortion circuit as claimed in claim 7 wherein said estimation-and-convergence algorithm causes said equalizer section to converge at said filter coefficients after processing a multiplicity of samples from said complex-return-data stream.

Claim 10 (original): A predistortion circuit as claimed in claim 7 wherein said

said estimation-and-convergence algorithm is responsive to said complex-forward-data stream and to said complex-return-data stream;

said complex-forward-data stream and said complex-return-data stream exhibit a forward-error level and a return-error

level, respectively, with said return-error level being greater than said forward-error level; and

said estimation-and-convergence algorithm controls a rate of convergence upon said filter coefficients to achieve a predetermined effective return-error level that is less than said return-error level.

Claim 11 (original): A predistortion circuit as claimed in claim 1 wherein said equalizer section implements a complex equalizer.

Claim 12 (original): A predistortion circuit as claimed in claim 1 wherein:

said complex-forward-data stream exhibits a forward resolution; and

said complex-return-data stream exhibits a return resolution less than said forward resolution.

Claim 13 (original): A predistortion circuit as claimed in claim 12 wherein said feedback section generates said complex-return-data stream so that said return resolution is at most four bits less than said forward resolution.

Claim 14 (canceled).

Claim 15 (original): A predistortion circuit as claimed in claim 1 additionally comprising a programmable delay element coupled between said complex-forward-data-stream source and said feedback section, said programmable delay element being configured to produce a delayed-complex-forward-data stream temporally aligned with said complex-return-data stream.

Claim 16 (original): A predistortion circuit as claimed in claim 15 wherein:

said complex-forward-data stream propagates through said predistortion circuit in response to a clock signal; and

said programmable delay element includes an integral section that delays at least a portion of said complex-forward-data stream by an integral number of cycles of said clock signal and includes a fractional section that delays said portion of said complex-forward-data stream by a fraction of a cycle of said clock signal.

Claim 17 (original): A predistortion circuit as claimed in claim 15 wherein:

said predistortion circuit additionally comprises a correlator having inputs coupled to said programmable delay element and to said feedback section and having an output coupled to said controller; and

said controller and said correlator are configured to implement an estimation-and-convergence algorithm to bring said delayed-complex-forward-data stream into temporal alignment with said complex-return-data stream.

Claim 18 (original): A predistortion circuit as claimed in claim 15 wherein said controller is configured to cause said programmable delay element to temporally align said delayed-complex-forward-data stream with said complex-return-data stream prior to causing said equalizer section to compensate for said frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components.

Claim 19 (original): A predistortion circuit as claimed in claim 15 wherein:

said equalizer section comprises an adaptive equalizer configured to determine filter coefficients that compensate for said frequency dependent quadrature gain and phase imbalance; and

said adaptive equalizer increases correlation between said delayed-complex-forward-data stream and said complex-return-data stream in determining said filter coefficients.

Claim 20 (original): A predistortion circuit as claimed in claim 1 wherein:

said analog-transmitter components include a band-pass filter which inserts a band-pass-filter delay; and

said predistortion circuit additionally comprises a phase rotator configured to rotate one of said complex-forward-data and complex-return-data streams relative to the other to compensate for said band-pass-filter delay.

Claim 21 (original): A predistortion circuit as claimed in claim 20 wherein said phase rotator is configured to implement an estimation-and-convergence algorithm to determine an amount of phase rotation that compensates for said band-pass-filter delay.

Claim 22 (original): A predistortion circuit as claimed in claim 20 wherein said controller is configured to cause said phase rotator to compensate for said band-pass-filter delay prior to causing said equalizer section to compensate for said frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components.

Claim 23 (original): A predistortion circuit as claimed in claim 20 wherein:

said equalizer section comprises an adaptive equalizer configured to determine filter coefficients that compensate for said frequency dependent quadrature gain and phase imbalance; and

said adaptive equalizer increases correlation between said complex-forward-data and complex-return-data streams after rotation of one of said complex-forward-data and complex-return-

data streams relative to the other in determining said filter coefficients.

Claim 24 (original): A predistortion circuit as claimed in claim 1 wherein said equalizer section includes a first equalizer configured to filter said complex-forward-data stream and a second equalizer configured to filter said complex-return-data stream.

Claim 25 (original): A predistortion circuit as claimed in claim 24 wherein:

said first equalizer is a non-adaptive equalizer programmed with forward-filter coefficients;

said second equalizer is a non-adaptive equalizer programmed with return-filter coefficients; and

said equalizer section additionally includes an adaptation engine selectively coupled to said first and second equalizers and configured to implement an estimation-and-convergence algorithm which determines said forward-filter and return-filter coefficients.

Claim 26 (original): A predistortion circuit as claimed in claim 24 wherein:

said analog-transmitter components include a power amplifier having an input and an output;

said feedback section has a first analog input adapted to receive a first RF-analog signal from said power amplifier input and a second analog input adapted to receive a second RF-analog signal from said power amplifier output;

said controller is configured to cause said feedback section to monitor said first RF-analog signal while adjusting said first equalizer to compensate for linear distortion at said input of said power amplifier, then cause said feedback section to monitor said second RF-analog signal while further adjusting

said first equalizer to compensate for linear distortion at said output of said power amplifier.

Claim 27 (original): A predistortion circuit as claimed in claim 26 wherein said controller is configured to, after adjusting said first equalizer to compensate for linear distortion at said output of said power amplifier, monitor said second RF-analog signal while adjusting said second equalizer to further compensate for linear distortion at said output of said power amplifier.

Claim 28 (original): A predistortion circuit as claimed in claim 27 wherein:

said first equalizer is adjusted to increase correlation between said second RF-analog signal and a first signal responsive to said complex-forward-data stream and having a first bandwidth; and

said second equalizer is adjusted to increase correlation between said second RF-analog signal and a second signal responsive to said complex-forward-data stream and having a second bandwidth wider than said first bandwidth.

Claim 29 (original): A predistortion circuit as claimed in claim 24 wherein:

said analog section includes a power amplifier which exhibits a gain; and

said predistortion circuit additionally comprises an adjustable attenuation circuit configured to compensate for said gain of said power amplifier and positioned to process said complex-return-data stream before filtering in said second equalizer.

Claims 30-65 (canceled).